In response to that Office Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel Claims 4, 6, 8, and 31-67, without prejudice or disclaimer of the subject matter presented therein.

Please amend Claims 3, 5, 7, 9-11, 13-17, and 30 to read as follows. A marked-up copy of the amended claims, showing the changes made thereto, is attached.

3. (Amended) A head substrate according to claim 2, wherein:

said recording execution means is adapted for executing the recording operation based on the recording image signal serially entered into one of said external connection terminals; and

A1

said common terminal wiring means allows at least one of the input of data into said memory access means and the output of data from said memory access means, using the same external connection terminal that serially inputs the recording image signal.

5. (Amended) A head substrate according to claim 2, wherein:

said recording execution means is adapted for executing the recording operation based on the recording image signal parallel entered into plurality of said external connection terminals; and

A2

said common terminal wiring means allows at least one of the parallel input of data into said memory access means and the parallel output of data from

A2 cont.

said memory access means, using the same external connection terminal that parallelly inputs the recording image signal.

7. (Amended) A head substrate according to claims 2 or 3, wherein:

said recording execution means includes a shift register which is reset by a reset signal externally entered into one of said external connection terminals and is adapted to temporarily hold and parallel output, at a timing corresponding to the clock signal, the recording image signal serially entered into another of said external connection terminals; and

A3

said common terminal wiring means is adapted for supplying said memory access means with the reset signal for said shift register, as said binary logic signal constituting said access permission signal.

9. (Amended) A head substrate according to claims 2 or 3, wherein:

said recording execution means includes a shift register which is adapted to be reset by a reset signal externally entered into one of said external connection terminals and then to temporarily hold and parallel output, at a timing corresponding to the clock signal, the recording image signal serially entered into another of said external connection terminals, and a latch circuit which is adapted to be reset by said reset signal and then to temporarily hold and output the recording image signal parallel outputted from said shift register; and

A4

said common terminal wiring means is adapted for supplying said memory access means with said reset signal as said binary logic signal constituting said access permission signal.

10. (Amended) A head substrate according to claims 2 or 3, wherein:

said recording execution means includes a shift register which is adapted to be reset by a reset signal externally entered into one of said external connection terminals and then to temporarily hold and parallel output, at a timing corresponding to the clock signal, the recording image signal serially entered into another of said external connection terminals, and a latch circuit which is adapted to temporarily hold and output the recording image signal parallel outputted from said shift register at a timing corresponding to a latch signal externally entered into still another of said external connection terminals; and

A4 cont.

said common terminal wiring means is adapted for supplying said memory access means with said latch signal as said binary logic signal constituting said access permission signal.

11. (Amended) A head substrate according to any of claims 1, 2, 3, and 5, wherein said recording execution means includes plural recording elements for recording the recording image signal parallel outputted from said latch circuit, corresponding to a recording pulse signal externally entered into one of said external connection terminals.

13. (Amended) A head substrate according to any of claims 2, 3, and 5, wherein said common terminal wiring means is adapted to supply said memory access means with the clock signal for said recording image signal, as a memory clock signal.

14. (Amended) A head substrate according to any of claims 2, 3, and 5, wherein:

said data memory means is means for executing both data writing and data readout as the memory access;

said memory access means is means for selectively executing either of data writing into and data readout from said data memory means corresponding to an externally entered mode switching signal; and

said common terminal wiring means is adapted for supplying said memory access means with the input signal to one of said external connection terminals as the mode switching signal.

15. (Amended) A head substrate according to any of claims 2, 3, and 5, wherein:

said recording execution means is adapted for receiving a driving electric power externally entered from one of said external connection terminals; and

said common terminal wiring means is adapted for supplying said memory access means with the driving electric power for said recording execution means.